

Design of Power Efficient and High Speed Carry Select Look Ahead Adder Using SP-D3L Logic

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Abstract— Minimizing area and power is the most challenging task in modern VLSI design. Adders are the most extensively used components in many integrated circuits; the design of power efficient high-speed data path logic systems forms the largest areas of research in VLSI system design. This paper presents a new vibrant logic named sp-D3L that conquers the speed limitations of D3L. Power consumption is considerably reduced by using the sp-D3L logic. Carry Select Look Ahead Adder is one of the fastest adders used in many data-processing circuits to perform fast arithmetic and logical functions. The simulation results show that there is reduction in the area and power consumption by using the sp-D3L logic.

Keywords- SP-D3L Logic, Area Optimization, Noise margin, Low powerCSLA.

I. INTRODUCTION

Design of power-efficient high-speed data path logic systems are one of the most taxing task in IC design industry. In digital adders, the speed of addition process is limited by the time required to propagate a carry. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input C_{in} and C_{out} then the final sum and carry are selected by the multiplexers. The performance of a full adder circuit depends on the type of design style used for execution as well as the logic function realized using the particular design style. For instance, a standard CMOS implementation allows circuits to achieve a reasonable power delay product with high noise margins, regular layout and relatively higher tolerance to process variations. Dynamic implementations on the other hand may yield an extremely fast design but end up paying higher costs in the overall power consumption. Data driven dynamic logic (D3L) and Split pre-charge data driven dynamic logic (sp-D3L) are the two design styles which will allow high performance dynamic circuit design without the additional power consumption in the clock distribution network. Thus these styles form interesting implementation strategies for realizing high performance, power-efficient full adders.

A carry-select adder takes the two input bits A and B and creates a true and partial sum from them. These go into a multiplexer which chooses the correct output based on the actual carry in. Carry-select adders are made by linking 2 adders together, one being fed a constant 0-carry, the other a constant 1-carry.

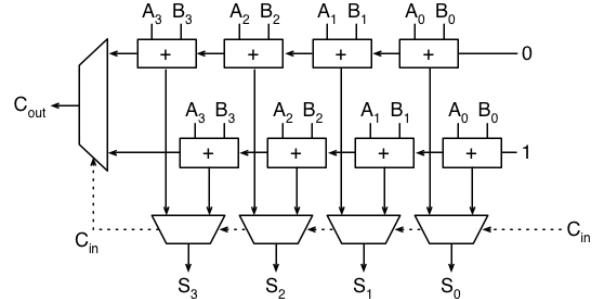


Figure 1. Structure of 14-Bit Carry Select adder

Fig.1 shows three full adder implementations in the recently proposed sp-D3L design style. Transistor sizing also plays a vital role in circuit performance along with the choice of logic function and implementation style. For dynamic adders it was observed that progressively sizing the rest of the transistors yielded the best power-delay Product while also maintaining drivability of the adder circuits. For the pass-transistor and transmission gate based adders, we have kept minimum sizes on all the transistors. This was found to be the best alternative since any performance advantage gained by upsizing the PMOS transistors in these circuits will increase the power consumption. While the speed advantage itself is off-set due to the inevitable use of buffers at the outputs of these adders. Hence, minimum sizing all the transistors yielded the best power-performance and area trade off.

The downside of the existing adders is the high power consumption because of the large number of transistors as well as the multiple paths to ground present in the sp-D3L implementations. With respect to the choice of logic function to implement, the full adder was observed to perform the best when implemented using the Propagate and Generate signals. This can be attributed to the fact that this function allows for smaller number of transistors stacked in series and shows the lowest capacitance at the output node. This shows that the capacitance at the output node forms the most critical component of the adder speed irrespective of the number of stages of circuits before getting the SUM and CARRY outputs.

II. RELATED WORK

Jiang, Sheraidah, Wang, and J. Chung have proposed that the 1-bit full adder is one of the most critical components of a processor, as it is used in the arithmetic logic unit, the floating-point unit, and address generation for cache or memory accesses. The static energy recovery full adder requires only 10 transistors to implement a full adder. Intensive simulation shows that the new adder has more than 26% in power savings over conventional 28-transistor CMOS adder.

Frustaci, Lanuzza, Zicari, Perri and Corsonello have proposed that the data-driven dynamic logic is very efficient under low-power constraints. It exploits a clock signal, uses a subset of the input data signals for pre-charging the dynamic node, thus avoiding the clock distribution network thereby power consumption is considerably reduced, but the pre-charge propagation path delay affects the speed performances. This technique leads to an EDP of 25 and 30% lower than standard dynamic domino logic and conventional D3L logics.

III. PROPOSED WORK

In the proposed work, different logic adders are introduced as shown in Fig.2 and Fig.3 to implement the carry select adder instead of using full adder. In each adder we have calculated the power and area. Two 4-bit ripple carry adders are multiplexed together, where the resulting carry and sum bits are selected by the carry-in. Since one ripple carry adder assumes a carry-in of 0, and the other assumes a carry-in of 1, the carry out of each 4-bit block is connected to the carry in of the next 4-bit block. When combined in this manner, 16-bit signed binary numbers can be computed. Subtraction is done using two's complement binary arithmetic. Table 1 shows the performance of different sp-D3L adder's styles.

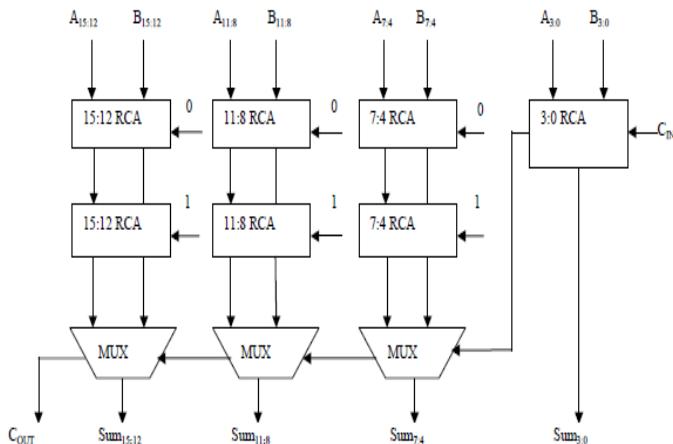


Figure 2. 16 Bit Carry select adder

TABLE I. PERFORMANCE ANALYSIS OF VARIOUS LOGIC ADDERS AND THEIR COMPARISON

Adder	No. of Transistors used	Power in mW	Area in nm
sp-D3L sum	45	38.45	6
sp-D3L carry	32	38.81	7
sp-D3L pg	48	38.09	7
16- bit CSLA	48	36.43	6
Ripple carry adder	48	40.17	7

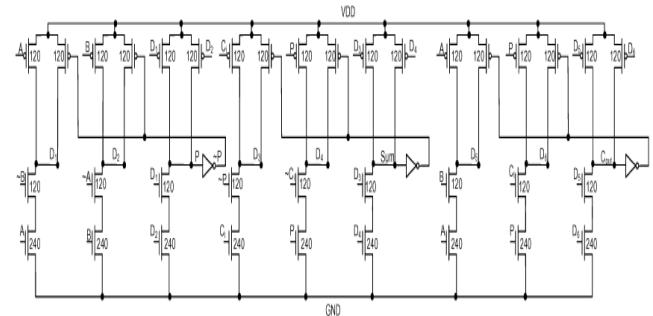


Figure 3. sp-D3L Logic Adder

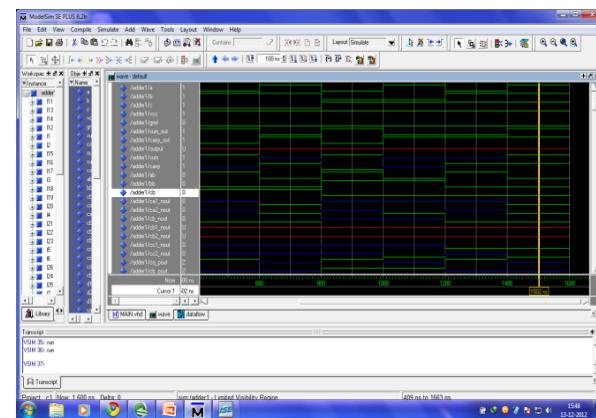


Figure 4. Simulation results of sp-D3L adder1

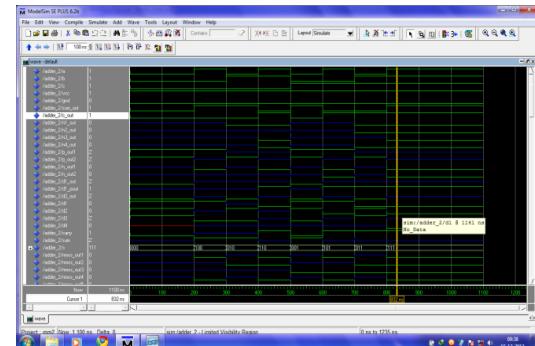


Figure 5. Simulation results of sp-D3L adder1

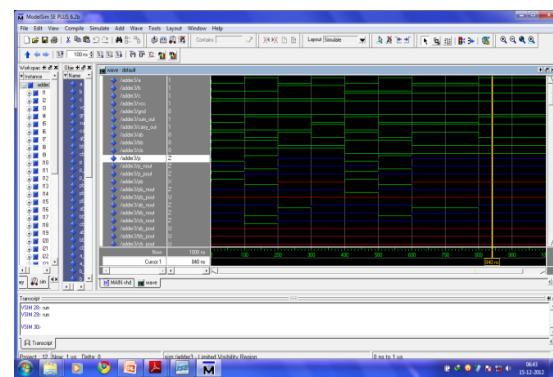


Figure 6. Simulation results of sp-D3L adder3

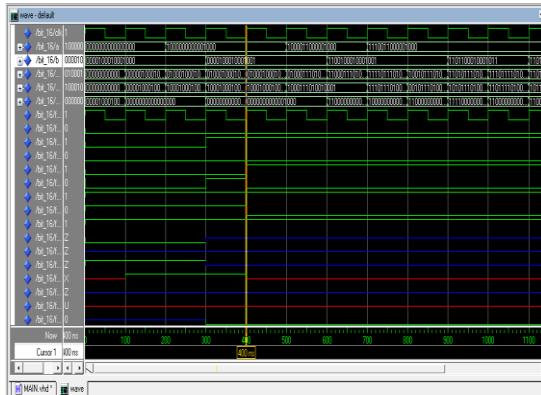


Figure 7. Simulation waveform of Proposed Carry Select Adder

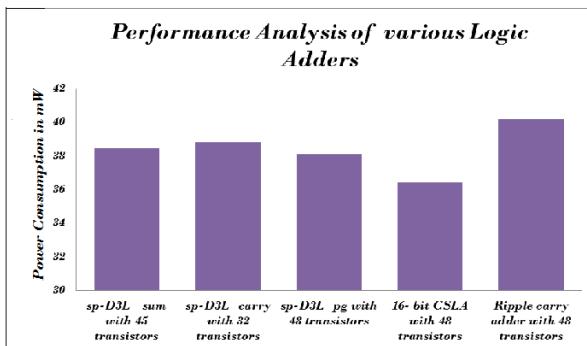


Figure 8. Power consumption of various logic adders

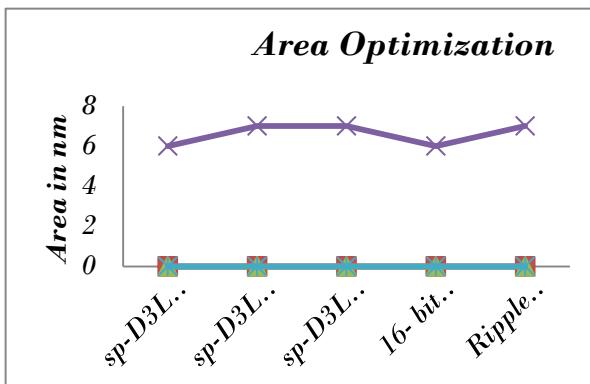


Figure 9. Area occupancy of different sp-D3L adders

IV. CONCLUSION

Using split-path implementation to implement full adder function yields better circuit performance in terms of both power efficiency as well as area optimization. These adders offer high computational speed than ripple carry adders. All the adders are designed using Very High Speed Integration Hardware Description Language; Xilinx Project Navigator 9.1i is used as a synthesis tool and ModelSim XE III 6.2i for simulation. Wherever there is need of smaller area and low power consumption, with acceptable increase in delay, these adders are suggested.

REFERENCES

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